REMARKS

Claims remaining in the present patent application are numbered 1-15. The rejections and comments of the Examiner set forth in the Office Action dated May 2, 2003 have been carefully considered by the Applicants. Applicants respectfully request the Examiner to consider and allow the remaining claims.

35 U.S.C. §112 Rejection

The present Office Action rejected Claims 6, 7, and 23 under 35 U.S.C. 112 for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Applicants have herein amended independent Claims 1 and 18 to have a single reference to an SPI device thereby avoiding the confusion to which SPI device, a first or second SPI device, the term "said SPI device" is referring.

35 U.S.C. §103 Rejection

The present Office Action rejected Claims 1-27 under 35 U.S.C. 103(a) as being unpatentable over Applicants' admission of prior art, in view of Gates (U.S. Patent No. 5,826,068). Applicants have reviewed the above cited references and respectfully submit that the present invention as recited in Claims 1-27, is neither anticipated nor

rendered obvious by Applicants' prior art admission alone or taken in combination with Gates.

Independent Claims 1 and 18

Applicants respectfully point out that currently amended independent Claim 1 and Claim 18 recite that the present invention includes, in part:

> [A] method of automatically detecting memory size comprising the steps of:
> * * *
> a) sending a READ command from a memory controller chip to a serial peripheral interface (SPI) device over an SPI interface for a first series of eight serial clock cycles;
> * * *
> d) automatically determining that said SPI device has memory addresses of up to nine bits when detecting the presence of a first non-zero value coming from said SPI device through said D-IO pin during a third series of eight serial clock cycles; and
> e) automatically determining that said SPI device has memory addresses of up to sixteen bits when detecting the presence of a first zero value at said D-IO pin during said third series of eight serial clock cycles and a second non-zero value coming from said SPI device through said D-IO pin during a fourth series of eight serial clock cycles. (Emphasis Added)

Embodiments of the present invention pertain to the automatic detection of memory size on a serial periphery interface (SPI) device that is electrically coupled to a memory controller. In particular, independent Claim 1, as currently amended, recites that a memory controller through

signals over a single data input/output (D-I/O) line can automatically determine the memory size of an SPI device that is coupled to the memory controller. Specifically, in independent Claims 1 and 18, an SPI device having memory addresses of up to nine bits is automatically determined when the memory controller detects the presence of a non-zero value coming from the SPI device over the D-I/O pin. Also, in independent Claims 1 and 18, an SPI device having memory addresses of up to sixteen bits is automatically determined when the memory controller detects the presence of a zero value in a third series of eight clock cycles coming over the D-I/O pin followed by a non-zero value over the D-I/O pin in a fourth series of eight clock cycles.

Applicants respectfully note that the Applicants' admitted prior art, taken alone or in combination with the Gates reference does not comprise nor suggest automatically determining and detecting a memory size of an SPI device by examining the signals received from the SPI device over a single D-I/O pin, as is presently claimed in amended independent Claims 1 and 18.

In contrast to independent Claim 1, as currently amended, of the present invention, the Gates reference pertains to a host adapter integrated circuit that contains data transfer modules, wherein the host adapter has a serial port that uses a single serial port pin to communicate with a

slave serial port input-output integrated circuit that interfaces to various resources that are included in a support circuit. However, the Gates reference does not teach a method of automatically detecting the memory size of an SPI device by examining the signals over a D-IO pin of a memory controller, as in the present invention of amended independent Claim 1.

In addition, the Applicants' admitted prior art states that an EEPROM varies in size and may consist of an address of one, two, three bytes, or larger (see page 2 lines 4-5). The admitted prior art does not suggest serial clock cycles, only that the address size of the EEPROM may be expressed in byte data units depending on the system being used.

It is suggested in the present Office Action that the Gates reference teaches a D-IO pin in a method of automatically detecting memory size. However, the statement is misleading in that Gates reference at most only indirectly teaches the use of the D-IO pin specifically for automatically detecting memory size of an SPI device.

In particular, the Gates reference does teach the use of a single bidirectional pin coupled to a serial port that is used to transfer information serially from and to an integrated circuit (see independent Claim 1 of the Gates reference). That is, the Gates reference is describing the

use of a bidirectional pin for the transfer of information. Specifically, a host adapter 240 has a single pin serial port that uses a single bidirectional pin for the transfer of information from and to a circuit, such as, a slave serial port input output circuit 254 in the support circuit 250 that is external to the host adapter 240 (see Figures 2A and 3, and summary, col. 2, lines 33-39 of the Gates reference). In particular, the slave serial port input-output integrated circuit 254 interfaces with various resources that are included in a support circuit 250. As a result, the host adapter 240 uses a single bidirectional pin for the transfer of information with a support circuit 250. Applicants argue that the host adapter only transfers information, and as such, does not provide the computational capacity to automatically determine the size of an SPI device.

On the other hand, the Gates reference does teach the detection of memory sizes of EEPRM 390 in the support circuit 250. That is, a portion of the support circuit 250 is capable of determining EEPROM memory size. Specifically, the Gates reference discloses that the ID-ESTAT detector 1375 within the support circuit 250 senses signals at a number of high address lines, such as, the first memory address line MA17 and a second memory address line MA16. In particular, the ID-ESTAT detector 1375 determines that the size of EEPROM 290 is 64 kilobytes when the ID-ESTAT detector 1375 senses that a low signal on MA17 and a low signal on MA16. Further,

the ID-ESTAT detector 1375 determines that the size of the EEPROM 290 is 128 kilobytes when the ID-ESTAT detector 1375 senses a high signal on MA16 and a low signal on MA17. Also, the ID-ESTAT detector 1375 determines that the size of the EEPROM 290 is 256 kilobytes when the ID-ESTAT detector 1375 senses a high signal on MA16 and a high signal on MA17. (See Figures 13 and 16, and col. 42, lines 17-22 of the Gates reference).

As a result, in the Gates reference, the ID-ESTAT detector 1375 in the support circuit 250, and not the host adapter 240, provides for the computing resources for determining and the detecting the memory size of an EEPROM 290. Moreover, the ID-ESTAT examines signals over at least two different lines, MA16 and MA17 in order to determine the memory size of the EEPROM 290. This teaching is however in stark contrast to embodiments of the present invention that are capable of automatically determining and detecting the memory size of an SPI device by examining serial signals over one line, the D-IO, as is presently claimed in amended independent Claims 1 and 18.

It is further argued that it would be obvious to combine the D-IO pin the Gates reference with the admitted prior art to provide reduced cost and complexity as well as increased applicability. However, since the bidirectional pin in the Gates reference discloses the transfer of information and not

specifically for the use of automatically determining the memory size of an SPI device, Applicants argue that the combined references do not teach the present method of automatically determining the memory size of an SPI device over a single D-IO line, as recited in amended independent Claims 1 and 18.

Thus, Applicants respectfully submit that the present embodiments as disclosed in independent Claim 1, as currently amended, are neither anticipated nor rendered obvious by the Gates reference, taken alone or in combination with the admitted prior art, and are in a condition for allowance. In addition, Applicants respectfully submit that Claims 2-10 which depend from independent Claim 1, as currently amended, are also in a condition for allowance as being dependent on an allowable base claim. Furthermore, Applicants respectfully submit that the present invention as disclosed in independent Claim 18, as currently amended, is neither anticipated nor rendered obvious by the Gates reference, taken alone or in combination with the admitted prior art, and is in a condition for allowance. In addition, Applicants respectfully submit that Claims 10-27 which depend from independent Claim 18, as currently amended, are also in a condition for allowance as being dependent on an allowable base claim.

Independent Claim 11

As for Claims 11-17, these constitute the SPI circuit for the methods disclosed in Claims 1-10 and 18-27. The arguments set forth in relation to independent Claims 1 and 18 of the previous section are applicable to independent Claim 11. As such, Applicants argue that the combined references of Gates and the admitted prior art do not teach or suggest the present method of automatically determining the memory size of an SPI device over a single D-IO line, as found in independent Claim 11.

As such, Applicants respectfully submit that the present invention as disclosed in independent Claim 11, as currently amended, is neither anticipated nor rendered obvious by the Gates reference, taken alone or in combination with the admitted prior art, and is in a condition for allowance. In addition, Applicants respectfully submit that Claims 12-17 which depend from independent Claim 11, as currently amended, are also in a condition for allowance as being dependent on an allowable base claim.

CONCLUSION

In light of the amendments and arguments presented herein, Applicants respectfully request reconsideration of the rejected Claims.

Based on the arguments presented above, Applicants respectfully assert that Claims 1-27 overcome the rejections of record. Therefore, Applicants respectfully solicit allowance of these Claims.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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